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NASA TECH BRIEF

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Single-Channel Digital Command-Detection System

The problem:

To provide a highly-reliable digital command-detection system which drains minimal power from an onboard power supply and eliminates nearly all of the bandpass and lowpass filters ordinarily used in conventional command systems.

The solution:

A single-channel command system fabricated entirely of highly-reliable digital logic elements; the system operates on binary pulse-code-modulated signals and derives internal synchronization from the data signal.

How it's done:

Deep-space command systems have converged on binary PCM transmission because of advantages in communication efficiency and handling of data. To solve the fundamental problem of PCM bit synchronization, Mariner spacecraft have used a transmitted reference scheme in which modulation power is shared between a data subcarrier and a sync subcarrier modulated by a pseudonoise (PN) code. Alternatively, methods may be used for deriving synchronization directly from the data to provide the best ultimate performance because the power allocated to data is at a maximum. The improved systems have been implemented with analog circuitry. Recent developments have led to a novel all-digital implementation of a detector which develops synchronization from the data signal by computing the cross-correlation of a command modulation signal with its expected forms in sequence and adjusts the detector phases in accordance with the correlation peaks. A shift register and serial adder are used to compute the correlations.

A noisy rf receiver ouput is correlated with a reference signal for a time of T_c seconds; if the largest correlation exceeds a threshold, indicating the presence of a command signal, the phase of the reference is adjusted to correspond to the phase of the correlation peak. The process of correlation must be done twice, once to establish subcarrier synchronization and once for bit synchronization; the serial approach simplifies required hardware. With T_c set equal to five bit times, the time required for serial establishment of the phase references is typically 80 bit times; a message prefix, 80 bit times long, is used to set and synchronize the command system prior to the actual command transmission.

The first signal transmitted (for 15 bit times of the message prefix) is the unmodulated subcarrier. The next 50 bits (typically) also are unmodulated subcarrier; for the next 15 bit times, the subcarrier is modulated by a bit sync. The detector correlates first with an unmodulated subcarrier for subcarrier sync, then uses the extra 50 bits of subcarrier to lock the subcarrier tracking loop to establish sync. (The duration of this portion of the prefix may be reduced, lengthened, or eliminated, depending upon the expected frequency offset of incoming subcarrier.) Finally, the detector correlates with bit sync to establish bit synchronization.

The correlation interval T_c is made equal to five bit times so that the sum of the rate of error incurred in detecting when the signal exceeds the threshold and the rate of error incurred in the selection of the

(continued overleaf)

proper phase is comparable to the probability of a data bit error. Allowable data error rates in a spacecraft command system are typically less than 10^{-5} per bit, and making the sync decision error rates similar in magnitude insures virtually certain success in the acquisition and detection process. The combination of the short acquisition time, 80 bits, with the high probability of acquisition, about $1-10^{-4}$, is a unique advantage of the digital system. The digital system tracks the subcarrier phase when in lock, and has a "lock detector"— a test which resets the system if the absolute value of accumulated correlations fails to pass a threshold. This decision is also made with error rate 10^{-5}.

The reliability advantage arises from the fact that all transistors downstream of the detector input analog-to-digital converter are either saturated or cut off, and thus the system operation does not depend on linear operation of components. The system using commercial low-power logic circuits can operate at PCM rates up to 512 bits/sec. At a normalized signal-to-noise ratio of 10 dB, the bit error rate is less than 10^{-5} and the acquisition error rate is less than 10^{-4}.

Note:

Requests for further information may be directed to:

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Reference: TSP 73-10342

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,701,894). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

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